REMARKS/ARGUMENTS

By this paper, Applicant responds to the Office Action of December 28, 2005 and respectfully requests reconsideration of the application. The shortened statutory period runs through March 28, 2006. Accordingly, this response is timely.

Claims 1-59 and 61-65 are now pending, a total of 64 claims. Claims 1, 2, 14, 22, 30, 40 and 55 are independent.

I. Paragraph 20: Claims 2, 9, 12 and 14 are Patentable Over Takusagawa '484

Paragraph 20 discusses portions of claim 2 in the context of Takusagawa '484. Claim 2 recites as follows

> 2. A method, comprising the step of:
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> for memory references generated as part of executing a stream of instructions on a computer, evaluating whether an individual memory reference of an instruction references a device having a valid memory address but that **cannot be guaranteed to be well-behaved**, based at least in part on an **annotation encoded in a segment descriptor**.

A. "Segment descriptor"

The Office Action does not designate any particular element of Takusagawa '484 to correspond to the "segment descriptor" of claim 2. Without a designation or an explanation of pertinence, it is difficult to interpret the Office Action.[1] Nonetheless, in an effort to advance prosecution, Applicant observes as follows.

"Segment descriptor" is a term of art. See Exhibits A and B. Takusagawa's "store-in" cache is not a "segment descriptor." Because the "segment descriptor" of claim 2 distinguishes Takusagawa '484, any rejection may be withdrawn.

Issues relating to an "annotation encoded in a segment descriptor" have been previously resolved. See Response of August 4, 2004, in paragraph spanning pages 17-18. It was agreed that "segment descriptor" is a term of art that distinguishes the TLB discussed in Cmelik '992.

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[1] 37 C.F.R. § 1.104(c)(2) requires that an Office Action designate portions of a reference relied on, and give a clear explanation of pertinence. Without a "designation" or "explanation," no rejection exists.

In light of that earlier agreement, and the similarities between Cmelik's TLB and Takusagawa's cache, it is difficult to discern the view expressed in this Office Action. If claim 2 is not allowed, Applicant requests a specific designation of a particular component (for example, by name or reference number) of any future reference thought to correspond to the "segment descriptor" of claim 2.

B. "Well-behaved Memory"

Paragraph 20 of the Office Action does not designate anything in Takusagawa '484 as corresponding to the "device having a valid memory address but that cannot be guaranteed to be well-behaved."

Issues relating to "well-behaved memory" were raised earlier, and resolved to the Examiner's satisfaction, by an explanation provided at pages 16-17 of the Response of August 4, 2004. There, Applicant drew the Examiner's attention to page 37-38 of the specification, which reads as follows:

> "Well-behaved memory" is a memory from which a load will receive the data last stored at the memory location. Non-well-behaved memory is typified by memory-mapped device controllers, also called "I/O space," where a read causes the memory to change state, or where a read does not necessarily return the value most-recently written, or two successive reads return distinct data.

"Well-behaved memory" is different than whether "a fault is detected."

If any future rejection is raised, Applicant requests a designation of a particular device in the reference relied on that "has a valid memory address" and that "cannot be guaranteed to be well-behaved." Applicant requests that the particular structure thought to correspond to the "device" and to the "address" each be designated by name or by reference number.

C. Conclusion: Claims 2, 9, 12 and 14 are Patentable Over Takusagawa '484

For reasons discussed in §§ I.A and I.B, claim 2 is patentable over Takusagawa '484, and the Office Action is too incomplete procedurally to raise any rejection over Takusagawa '484.

Claim 14 recites similar language, and is patentable for similar reasons.

Claims 9 and 12 are dependent on claim 2, and patentable therewith. In addition, claims 2 and 9 recite further limitations that distinguish Takusagawa '484. For example, "an address in I/O space of the computer" is a term of art (see specification, p. 37, line 5, page 117, line 2, etc.).

Takusagawa does not disclose that his store-in cache memory is a "device having a valid memory address ... in an I/O space of the computer"). If any rejection is thought to apply, Applicant requests a specific designation of the "address" of the component, and of the "I/O space." Claim 12 recites a "segment descriptor and "segment register." These are established terms of art, as shown in Exhibits A and B. A "valid register" in a write-in cache is not a "segment register."

Applicant respectfully requests that, in any further Office Action, the Examiner take care to address all claim limitations – and to both "designate" portions of the references relied on, and give a clear explanation of pertinence, as required by 37 C.F.R. § 1.104(d)(2).

II. Paragraph 12: Claim 3 is Patentably Distinct from Claim 7 of the '379 Patent

The Office Action raises a "double patenting" issue based on claims 2+3 of this application and 4+7 of the '379 patent. The Office Action is rather confusing: the views stated in this Office Action are inconsistent with views stated in earlier Office Actions.

First, the Office Action misidentifies the differences between the claims. The claims differ to at least the extent underlined:

Instant claim 2+3	'379 Patent Claims 4+7
2. A method, comprising the step of:	4. A method, comprising the steps of:
for memory references generated as part of executing a stream of instructions on a computer, evaluating whether an individual memory reference of an instruction references a device having a valid memory address but that cannot be guaranteed to be well-behaved, based at least in part on an annotation encoded in a segment descriptor.	
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
3. A method of claim 2, further comprising the step of:	7. The method of claim 4, further comprising the steps of:

if the reference cannot be guaranteed to be well-behaved, re-executing the instruction in an alternative execution mode.	evaluating whether an individual memory reference of an instruction references a device that cannot be guaranteed to be well-behaved, and if the reference cannot be guaranteed to be well-behaved, re-executing the instruction in an alternative execution mode.

The Office Action only addresses some of these differences, not all of them. Without a consideration of all the differences, it is difficult to respond directly.

Second, it was previously acknowledged that "an annotation encoded in a segment descriptor" is a non-obvious difference. Compare Response of 8/4/2004, paragraph spanning pp. 17-18 (noting that "segment descriptor" distinguishes Cmelik '992), to Office Action of 12/30/04 (agreeing that any rejection based on Cmelik '992 was withdrawn). The Examiner's attention has been drawn to this difference on a number of occasions (Response of 9/30/05, §§ VI(A)(2) at pp. 7-8, sections "Second Error," "Third Error," "Fourth Error," and "Fifth Error;" Response of 2/28/05 at p. 3, section "Fourth," paragraphs (b) and (c)). Until an Office Action "answers all material traversed" as required by MPEP § 707.07(f) and states a view on this issue, the 12/28/05 Office Action is procedurally insufficient to raise any rejection. At this point, Applicant can only respectfully ask once again that the "annotation encoded in a segment descriptor" language of the claims be considered.

Third, the Office Action equates determining whether memory is "well-behaved" with whether a fault is detected or not. "Well-behaved memory" is different than whether a fault is detected – see § I.B at page 3, above. The Office Action does not suggest that Takusagawa '484 determines whether memory is "well-behaved." This is a non-obvious difference between the claims.

Fourth, the Office Action picks and chooses bits and pieces of Takusagawa '484 for piecemeal substitution into the '379 claims. The Office Action is simply silent on the interrelationships recited in the claim – it makes no showing that it would be obvious to combine the '379 claims plus bits and pieces of Takusagawa '484, to obtain the interconnections recited in claims 2+3. This is not permitted. *Ex parte Beuther*, 71 USPQ2d 1313, 1316 (Bd. Apt. App. & Interf. 2003) (it is impermissible "to pick, choose, and combine various portions of the disclosure

not directly related to each other by the teachings of the reference"). The obviousness analysis of the Office Action is faulty, and fails to make a genuine showing of obviousness.

Fifth, the Office Action relies on Takusagawa '484, col. 1, lines 39-42 for "motivation to combine." Takusagawa '484 states something quite different. Col. 1, lines 39-42 provides motivation to modify or combine "the foregoing," that is, the conventional store-in cache described at col. 1 lines 7-36. There is no showing in the Office Action of "motivation to combine" with the unrelated subject matter of the '379 claims.

No double patenting rejection is raised, and none is warranted.

III. Paragraph 15: Claims 22 and 30 Are Patentably Distinct From Claim 8 of the '379 Patent

Claims 22 and 30 of this application differ from claims 4+8 of the '379 patent to at least the extent underlined below:

Instant claim 22	'379 Patent Claims 4+8
22. A method, comprising the steps of:	4. A method, comprising the steps of:
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
	8. The method of claim 4, further comprising the steps of:
while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second representation in a second instruction set architecture, distinguishing individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory device(s);	while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second instruction set architecture, using the recording to distinguish memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory;
while executing the second representation, identifying a load that was believed at translation time to be directed to well-behaved memory but that at execution time is found to be directed to non-well-behaved memory, based at least in part on an annotation encoded in a segment descriptor, and aborting the identified memory load; and	while executing the translation into the second instruction set architecture, identifying loads that were believed at translation time to be directed to well-behaved memory but that at execution are found to be directed to non-well-behaved memory, and aborting the identified memory load;

based at least in part on the identifying, re-executing at least a portion of the translated segment of the program in the first instruction set.	re-executing at least a portion of the translated segment of the program in the first instruction set.

Instant claim 30	**'379 Patent Claims 4+8**
30. An apparatus, comprising:	4. A method, comprising the steps of:
	issuing a successful memory reference from a computer CPU to a bus;
	recording in a storage of the computer whether a device accessed over the bus by the memory reference is well-behaved memory or not-well-behaved memory.
	8. The method of claim 4, further comprising the steps of:
a binary translator programmed to translate at least a segment of a binary representation of a program from a first instruction set architecture to a second representation in a second instruction set architecture, distinguishing individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory; and	while translating at least a segment of a binary representation of a program from a first instruction set architecture to a second instruction set architecture, using the recording to distinguish memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory;
instruction execution circuitry designed to execute the translated program in the second representation, and to identify, based at least in part on an annotation encoded in a segment descriptor, memory loads that were believed at translation time to be directed to well-behaved memory but that at execution time are found to be directed to non-well-behaved memory, and to abort the identified memory load.	while executing the translation into the second instruction set architecture, identifying loads that were believed at translation time to be directed to well-behaved memory but that at execution are found to be directed to non-well-behaved memory, and aborting the identified memory load;
	re-executing at least a portion of the translated segment of the program in the first instruction set.

Paragraphs 14 and 15 of the Office Action do not purport to reject either claim 22 or 30.

No rejection exists. Nonetheless, in a good faith effort to advance prosecution, Applicant notes:

a) Paragraphs 14 and 15 of the Office Action are silent on the language "segment descriptor" that has been noted in Applicant's two previous papers. A prior Office Action conceded that "segment descriptor" is a non-obvious difference over the prior art. See discussion item "Second" at page 5, above.

b) the "'379 Patent teachings" (Office Action of 12/28/05 at page 8, lines 17-18 and page 9, line 14-15) may not be relied upon. MPEP § 804(B)(1) ("the disclosure of the patent may not be used as prior art.")

c) The "motivation to combine" stated in the Office Action is incorrect. See discussion item "Fifth" at page 6, above.

Prosecution cannot advance when several successive Office Actions have been silent on the same issue. The Federal Circuit has requested that the Examiner either state a view, supported by evidence, or allow the application. *In re Oetiker*, 977 F.2d 1443, 1445-46, 24 USPQ2d 13443, 1444 (Fed. Cir. 1992) ("the examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability. ... If examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent." emphasis added).

Applicant requests allowance of any claim for which no complete statement of a rejection (as provided in MPEP § 804(B)(1)) is provided.

IV. Paragraph 8: Claim 14 is Not a "Single Means Claim"

Claim 14 recites as follows:

> 14. (previously presented) A computer, comprising:
>
> instruction execution circuitry designed to evaluate, based at least in part on an annotation encoded in a segment descriptor, whether an individual memory-reference instruction, or an individual memory reference of an instruction, references a device with a valid memory address that cannot be guaranteed to be well-behaved.

MPEP § 2164.08(c) states that a "single means claim" can only exist where a claim recites a "means" element. Claim 14 recites no "means" element. It is a "zero means" claim. No rejection is warranted.

V. Paragraphs 9, 10, 11 – Claims 2 and 14 are "Complete" As Required by Law

Claims 2 and 14 were drafted in reliance on PTO policy as set forth in MPEP § 2172.01.

All elements of claims 2 and 4 are interconnected. None have a "gap between" them. To raise a rejection based on § 2172.01, an Office Action must identify two elements that are in the claim, and show that there is no interconnection. The Office Action fails to mention any relevant facts that might support a rejection.

MPEP § 2172.01 only authorizes a rejection when the "the specification or [ ] other statements of record" state that certain elements are "essential." Personal judgment is not a permissible basis to determine that an element is "essential." The Office Action points to no statements in "the specification or in other statements of record" to establish that any element is "essential." The Office Action is too incomplete to raise any rejection.

The Office Action states a different rationale, not authorized by MPEP § 2172.01. The rationale stated in the Office Action was abolished fifty years ago. *In re Gustafson*, 331 F.2d 905, 141 USPQ 585 (CCPA 1964). A recent decision of the Federal Circuit, *Carl Zeiss Stiftung v. Renishaw PLC*, 945 F.2d 1173, 1180-81, 20 USPQ2d 1094, 1100 (Fed. Cir. 1991) confirms that claims may not be rejected on the grounds stated in the Office Action (emphasis added, citations and quotations omitted):

> The district court misapplied the claim definiteness requirement in holding claim 3 to be invalid for failure to claim the subject matter regarded as the invention. Focusing on the fact that claim 3 omits any electrical circuitry or other signaling means, the court concluded that the claim "does not describe [the patentee's] invention." ... Stating that "the arbitrary presentation of part of an invention does not constitute a claim of a valid invention," the court essentially ruled that [the patentee] cannot claim a part of his invention separate from the rest. This reasoning is legal error.
>
> It has long been held, and we today reaffirm, that it is entirely consistent with the claim definiteness requirement of the second paragraph of section 112, to present "subcombination" claims, drawn to only one aspect or combination of elements of an invention that has utility separate and apart from other aspects of the invention. As one of our predecessor courts stated, "it is not necessary that a claim recite each and every element needed for the practical utilization of the claimed subject matter," as it is "entirely appropriate, and consistent with § 112, to present claims to only [one] aspect." Thus, the holding of invalidity that rests on a conclusion of lack of claim definiteness is legally incorrect.

The Office Action states that "it is unclear as to how..." (Office Action of 12/28/05 at p. 4). The Federal Circuit has specifically addressed this line of reasoning, and rejected it:

> The district court objected that the claims are not self-contained in that they do not explain that "video display information is produced by the controller." We agree that the claims are not a self-contained explanation of every step. That is not the role of claims.
>
> The purpose of claims is not to explain the technology or how it works, but to state the legal boundaries of the patent grant. A claim is not "indefinite" simply because it is hard to understand when viewed without benefit of the specification.

S3, Inc. v. nVidia Corp., 259 F.3d 1364, 1369, 59 USPQ2d 1745, 1748 (Fed. Cir. 2001) (emphasis added).

Paragraphs 9, 10 and 11 are without legal basis, and raise no rejection.

VI. Paragraphs 16-19: Claims 2 and 14 Recite § 101 Patentable Subject Matter

Claims 2 and 14 are patentable subject matter – they satisfy each of the three steps of analysis set out in the Office's Interim Subject Matter Guidelines (Oct 26, 2005). There is no genuine question that claim 2 is a "process or improvement thereof," and claim 14 is a "machine or improvement thereof." Neither claim is directed to a "mathematical algorithm" or mental process or anything else recognized to be an "abstract idea" (Interim Guidelines, p. 23). Both claims require practical machines, for example, by "executing a stream of instructions on a computer," a "memory reference" to a "device," and a "segment descriptor" – these are neither "abstract" nor "natural."

The Office Action considers "transformation of data" as the sole test for patentability. But the Interim Guidelines specify that "practical application" is the relevant test, and that "transformation of data" is only one of several "various ways" to establish "practical application." The specification states practical applications. *E.g.*, § VIII.B, pp. 135-36. Without a showing that one skilled in the art would question the practical application stated in the specification, MPEP § 2107.02(III)(A), no rejection exists.

Paragraph 19 misquotes the cases and MPEP section it relies on. Under older cases, and MPEP § 2106(IV)(B)(1)(a), a program or data structure might require a computer-readable medium. But no authority supports the Office Action, that a "computer," as recited in claim 14, or a method that requires hardware, as in claim 2, requires a program.

VII. Conclusion

In view of these remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. In the event that any extension of time is required, Applicant

petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-20-4009.

Respectfully submitted,

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Dated: March 28, 2006

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